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This listing of claims will replace all prior versions, and listings, of claims in the application:

- 1 Claim 1 (previously presented): A method of operating a receiver apparatus to generate soft values from a set of complex values communicated to said receiver apparatus, the method comprising operating said apparatus to perform the steps of:
 - 5 a) receiving a first set of complex values, said first set of complex values being received complex symbol values obtained from signals communicated over a channel;
 - 8 b) receiving a set of soft bits, said soft bits corresponding to said complex symbol values;
 - 10 c) performing a complex multiplication operation on each of at least some of said first set of complex values to generate at least some elements of a second set of complex values, the multiplication operation performed on each individual one of said set of at least some of said first set of complex values including multiplying said individual complex values by a complex value determined from at least some of said soft bits;
 - 17 d) summing said complex values in said second set of complex values to generate a complex sum, said complex sum being a complex value;
 - 20 e) generating a third set of complex values, said third set having the same number of elements as said first set of complex values, by separately subtracting from said complex sum one of said second set of complex values, each separate subtraction generating one of said third set of complex values; and
 - 25 f) multiplying each element of said first set of complex values with the conjugate of a complex value from said third set to generate a fourth set of complex values, said fourth set having the same number of elements as the first and second sets, said complex values in said fourth set being generated soft symbol values.

1 Claim 2 (original): The method of claim 1, wherein said received
2 set of soft values is generated from the output of a decoder.

1 Claim 3 (original): The method of claim 1, wherein said separate
2 subtractions performed in said step of generating a third set of
3 complex values are performed sequentially.

1 Claim 4 (original): The method of claim 1, wherein there are at
2 least two soft bits per received complex symbol value.

1 Claim 5 (original): The method of claim 1, wherein there are at
2 least 3 soft bits per received complex symbol value.

1 Claim 6 (original): The method of claim 1, wherein one of the
2 received complex symbol values is unmodified in phase by said
3 step of performing said complex multiplication operation on each
4 of at least some of said first set of complex values.

1 Claim 7 (original): The method of claim 6, wherein said complex
2 symbol value that is unmodified in phase occurs in a preselected
3 location within the first set of received complex symbol values.

1 Claim 8 (original): The method of claim 6, wherein for said
2 complex symbol value that is unmodified in phase, the
3 multiplication is known and independent of soft bits.

1 Claim 9 (original): The method of claim 6, wherein said complex
2 symbol value that is unmodified in phase is a pilot symbol
3 value.

1 Claim 10 (original): The method of claim 6, wherein said complex
2 symbol value that is unmodified in phase is a known symbol value
3 representing a pseudo pilot symbol.

1 Claim 11 (original): The method of claim 1, further comprising:
2 performing a soft input soft output decoding operation on
3 said soft symbol values to generate additional soft bits.

1 Claim 12 (original): The method of claim 11, further comprising:
2 using said generated additional soft bits to process
3 another set of complex symbol values.

1 Claim 13 (original): The method of claim 11, wherein said soft
2 input soft output decoding operation is performed by a low
3 density parity check decoder.

1 Claim 14 (original): The method of claim 11, wherein said soft
2 input soft output decoding operation is performed by a turbo
3 decoder.

1 Claim 15 (original): The method of claim 1, wherein said first
2 set of complex symbol values are produced by an OFDM modulated
3 communications system.

1 Claim 16 (original): The method of claim 1, further comprising:
2 storing each of the generated second set of complex symbol
3 values for a predetermined time, said subtracting using symbol
4 values from said second set which have been stored for said
5 predetermined time.

1 Claim 17 (original): The method of claim 16, further comprising:
2 storing each of the first set of complex symbol values for
3 a second predetermined time, said second predetermined time
4 being longer than the first predetermined time; and
5 wherein said first complex symbol values multiplied with
6 said third complex symbol values have been delayed for said
7 second predetermined time.

1 Claim 18 (original): The method of claim 5, wherein said complex
2 multiplication operation on each of at least some of said first
3 set of complex values is performed by performing no more than
4 two shift operations and no more than one addition operation.

1 Claim 19 (original): The method of claim 1, wherein the
2 communication signal is block-coherent communication signal.

1 Claim 20 (original): The method of claim 1, wherein one of the
2 received complex symbol values is modified in phase by said step
3 of performing said complex multiplication operation on each of
4 at least some of said first set of complex values by a fixed
5 preselected amount.

1 Claim 21 (original): The method of claim 20, wherein said
2 complex symbol value that is modified in phase by a fixed
3 preselected amount occurs in a preselected location within the
4 first set of received complex symbol values.

1 Claim 22 (original): The method of claim 20, wherein for said
2 complex symbol value that is modified in phase by a fixed
3 preselected amount, the multiplication is known and independent
4 of soft bits.

1 Claim 23 (previously presented): A apparatus for generating soft
2 values from a set of complex values, the apparatus comprising:
3 a first complex multiplier including:
4 i) a first input for receiving a first set of complex
5 values, said first set of complex values being
6 received complex symbol values obtained from signals
7 communicated over a channel;
8 ii) a second input for receiving a set of soft bits,
9 said soft bits corresponding to said complex symbol
10 values; and

11 iii) circuitry for performing a complex multiplication
12 operation on each of at least some of said first set
13 of complex values to generate at least some elements
14 of a second set of complex values, the multiplication
15 operation performed on each individual one of said set
16 of at least some of said first set of complex values
17 including multiplying said individual complex values
18 by a complex value determined from at least some of
19 said soft bits;

20 a summer coupled to said first complex multiplier for
21 summing said complex values in said second set of complex values
22 to generate a complex sum, said complex sum being a complex
23 value;

24 means for generating a third set of complex values, said
25 third set having the same number of elements as said first set
26 of complex values, by separately subtracting from said complex
27 sum one of said second set of complex values, each separate
28 subtraction generating one of said third set of complex values;
29 and

30 means for multiplying each element of said first set of
31 complex values with the conjugate of a complex value from said
32 third set to generate a fourth set of complex values, said
33 fourth set having the same number of elements as the first and
34 second sets, said complex values in said fourth set being
35 generated soft symbol values.

1 Claim 24 (original): The apparatus of claim 23, further
2 comprising:

3 a decoder which generates soft output values, said decoder
4 being coupled to said first input of said first complex
5 multiplier.

1 Claim 25 (original): The apparatus of claim 23, wherein said means
2 for generating a third set of complex values, includes a delay

3 line for delaying complex values included in said second set of
4 complex values and a subtractor coupled to said delay line.

1 Claim 26 (original): The apparatus of claim 23, wherein there
2 are at least two soft bits per received complex symbol value.

1 Claim 27 (original): The apparatus of claim 23, wherein said
2 means for multiplying each element of said first set of complex
3 values with the conjugate of a complex value from said third set
4 to generate a fourth set of complex values includes:

5 a conjugate circuit; and
6 a second complex multiplier.

1 Claim 28 (new): An apparatus comprising:
2 a processor for use in a receiver apparatus to generate
3 soft values from a set of complex values communicated to said
4 receiver apparatus, the processor configured to:
5 a) receive a first set of complex values, said first
6 set of complex values being received complex symbol values
7 obtained from signals communicated over a channel;
8 b) receive a set of soft bits, said soft bits
9 corresponding to said complex symbol values;
10 c) perform a complex multiplication operation on each
11 of at least some of said first set of complex values to generate
12 at least some elements of a second set of complex values, the
13 multiplication operation performed on each individual one of
14 said set of at least some of said first set of complex values
15 including multiplying said individual complex values by a
16 complex value determined from at least some of said soft bits;
17 d) sum said complex values in said second set of
18 complex values to generate a complex sum, said complex sum being
19 a complex value;
20 e) generate a third set of complex values, said third
21 set having the same number of elements as said first set of

22 complex values, by separately subtracting from said complex sum
23 one of said second set of complex values, each separate
24 subtraction generating one of said third set of complex values;
25 and

26 f) multiply each element of said first set of complex
27 values with the conjugate of a complex value from said third set
28 to generate a fourth set of complex values, said fourth set
29 having the same number of elements as the first and second sets,
30 said complex values in said fourth set being generated soft
31 symbol values.

1 Claim 29 (new): A computer readable medium embodying machine
2 executable instructions for controlling a receiver apparatus to
3 implement a method of generating soft values from a set of
4 complex values communicated to said receiver apparatus, the
5 method comprising operating said apparatus to perform the steps
6 of:

7 a) receiving a first set of complex values, said first set
8 of complex values being received complex symbol values obtained
9 from signals communicated over a channel;

10 b) receiving a set of soft bits, said soft bits
11 corresponding to said complex symbol values;

12 c) performing a complex multiplication operation on each of
13 at least some of said first set of complex values to generate at
14 least some elements of a second set of complex values, the
15 multiplication operation performed on each individual one of
16 said set of at least some of said first set of complex values
17 including multiplying said individual complex values by a
18 complex value determined from at least some of said soft bits;

19 d) summing said complex values in said second set of
20 complex values to generate a complex sum, said complex sum being
21 a complex value;

22 e) generating a third set of complex values, said third set
23 having the same number of elements as said first set of complex

24 values, by separately subtracting from said complex sum one of
25 said second set of complex values, each separate subtraction
26 generating one of said third set of complex values; and

27 f) multiplying each element of said first set of complex
28 values with the conjugate of a complex value from said third set
29 to generate a fourth set of complex values, said fourth set
30 having the same number of elements as the first and second sets,
31 said complex values in said fourth set being generated soft
32 symbol values.

1 Claim 30 (new): A apparatus for generating soft values from a
2 set of complex values, the apparatus comprising:

3 first complex multiplier means including:

4 i) first input means for receiving a first set of
5 complex values, said first set of complex values being
6 received complex symbol values obtained from signals
7 communicated over a channel;

8 ii) second input means for receiving a set of soft
9 bits, said soft bits corresponding to said complex
10 symbol values; and

11 iii) means for performing a complex multiplication
12 operation on each of at least some of said first set
13 of complex values to generate at least some elements
14 of a second set of complex values, the multiplication
15 operation performed on each individual one of said set
16 of at least some of said first set of complex values
17 including multiplying said individual complex values
18 by a complex value determined from at least some of
19 said soft bits;

20 summer means coupled to said first complex multiplier means
21 for summing said complex values in said second set of complex
22 values to generate a complex sum, said complex sum being a
23 complex value;

24 means for generating a third set of complex values, said
25 third set having the same number of elements as said first set
26 of complex values, by separately subtracting from said complex
27 sum one of said second set of complex values, each separate
28 subtraction generating one of said third set of complex values;
29 and

30 means for multiplying each element of said first set of
31 complex values with the conjugate of a complex value from said
32 third set to generate a fourth set of complex values, said
33 fourth set having the same number of elements as the first and
34 second sets, said complex values in said fourth set being
35 generated soft symbol values.

1 Claim 31 (new): The apparatus of claim 30, further comprising:
2 decoder means which generates soft output values, said
3 decoder means being coupled to said first input means of said
4 first complex multiplier means.

1 Claim 32 (new): The apparatus of claim 30, wherein said means
2 for generating a third set of complex values, includes delay
3 line means for delaying complex values included in said second
4 set of complex values and subtractor means coupled to said delay
5 line means.

1 Claim 33 (new): The apparatus of claim 30, wherein there are at
2 least two soft bits per received complex symbol value.

1 Claim 34 (new): The apparatus of claim 30, wherein said means
2 for multiplying each element of said first set of complex values
3 with the conjugate of a complex value from said third set to
4 generate a fourth set of complex values includes:
5 conjugate means; and
6 second complex multiplier means.